
To: Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

From: **William J. Stoffel**
Reg no. 39,390
Customer no. 30,402

1735 Market St - Ste A455
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Work 215-670-2455
Fax 267-200-0730

Subject:	Request for Certification of correction
PATENT NO	US 7,064,358 B2

Subject: Request for Certification of correction
PATENT NO US 7,064,358 B2
ISSUED Jun. 20, 2006
Serial No. 10/743,596
Attorney Docket: CS03-036

File date: Dec. 22, 2003

Inventor: Manna, Indrajit et al.

Title : TRIGGERED BACK-TO-BACK DIODES FOR ESD PROTECTION IN TRIPLE-WELL CMOS PROCESS

SUPPLEMENTAL REQUEST FOR CERTIFICATION OF CORRECTION

Dear Sir:

Applicant requests this **Supplemental Certificate Of Correction** for the above mentioned patent to **REPLACE** the previous corresponding first Request for Certificate of Correction dated October 20, 2006- received by the uspto mail room on Oct 24, 2006,

This supplemental certificate of correction corrects one change the first request for correction at **Claim 14, Col. 9, Line 22,** i.e. that "p-well" is replaced with --N-well -- after ***"the deep"*** (emphasis added) and that this is supported by Applicant's reply to the office action dated June 2, 2005 which correctly shows *"N-well"* (emphasis added) at this line. This change is in the bolded paragraph on page 3 below.

CERTIFICATE OF MAILING OR FACSIMILE TRANSMISSION
I hereby certify that this correspondence is being : [_] FAXED to the central facsimile number of patent and trademark office at the following number **(571) 273-8300** or [_] deposited with the United States Postal Service as first class mail in an envelope addressed to: Attn: Certificate of Correction branch, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450; on the date below.
/William J. Stoffel REG # 39,390/ William J. Stoffel date November 29, 2006 Customer No. 30402

Dear Madam and Sir:

- The above patent contains significant errors as indicated on the attached certificate of correction form (SB44) (submitted in duplicate). There errors arose at the respective places in the application file as indicated below.
- Such errors arose through the fault of the Patent and Trademark Office, therefore patentee requests that the Certificate be issued at no cost.
- Please note several errors appear to have been made printing the claims from the Applicant's reply to the office action dated June 2, 2005 (Ex parte Quayle) and also see the originally filed application.

- **Specifically,** in issued Claim 1, Col. 8, line 15, please replace "p-well" with -- N-well—before "functioning". For support see the Applicant's reply to the office action dated June 2, 2005 (Ex parte Quayle), page 3, (claim 1) which correctly shows "N-well functioning" at this line. Also see the originally filed application. This appears to have been erroneously printed by the patent office.

- **Specifically,** in issued Claim 9, Col. 8, line 58, please replace "grounded-sate" with --grounded-gate—before "nMOS". For support see the Applicant's reply to the office action dated June 2, 2005 (Ex parte Quayle), page 4, (claim 9) which correctly shows "grounded-gate" at this line. Also see the originally filed application. This appears to have been erroneously printed by the patent office.

- Specifically, in issued Claim 14, Col. 9, line 16, please add --pad-- after "first I/O". For support see the Applicant's reply to the office action dated June 2, 2005 (Ex parte Quayle), page 5, (claim 14) which correctly shows "first I/O pad" at this line. Also see the originally filed application. This appears to have been erroneously printed by the patent office.

- **Specifically, in issued Claim 14, Col. 9, line 22, please replace "p-well" with --N-well-- after "the deep". For support see the Applicant's reply to the office action dated June 2, 2005 (Ex parte Quayle), page 5 (claim 14) which correctly shows "N-well" at this line. Also see the originally filed application. This appears to have been erroneously printed by the patent office.**

- Specifically, in issued Claim 20, Col. 9, line 50, please replace "fanning" with --forming-- before "a RC network". For support see the Applicant's reply to the office action dated June 2, 2005 (Ex parte Quayle), page 6 (claim 20). Also see the originally filed application. This appears to have been erroneously printed by the patent office.

- Specifically, in issued Claim 26, Col. 10, line 24, please replace "p-well" with --N-well-- before "functioning". For support see the Applicant's reply to the office action dates June 2, 2005 (Ex parte Quayle), page 7 (claim 26). Also see the originally filed application. This appears to have been erroneously printed by the patent office.

- Specifically, in issued Claim 33, Col. 11, line 4, please replace "p-well" with --N-well-- before "functioning". For support see the Applicant's reply to the office action dates June 2, 2005 (Ex parte Quayle), page 9 (claim 33). Also see the originally filed application. This appears to have been erroneously printed by the patent office.

CONCLUSION

In conclusion, issuance of the certificate of correction is respectfully requested.

This Supplement certificate of correction **REPLACES** the previous corresponding first Request for Certificate of Correction dated October 20, 2006- received by the USPTO mail room on Oct 24, 2006.

The representative requests that the patent office do not issue the first Request for Certificate of Correction dated October 20, 2006- received by the uspto mail room on Oct 24, 2006.

It is requested that the Examiner telephone the undersigned attorney at (215) 670-2455 should there be anyway that we could help to expedite issuance of the Certificate of Correction.

Charge to Deposit Account

The Commissioner is hereby authorized to apply any fees or credits in this case, which are not already covered by check or credit card, to Deposit Account No. 502018 referencing this attorney docket. The Commissioner is also authorized to charge any additional fee under 37 CFR §1.16 and 1.17 to this Deposit Account.

Respectfully submitted,

/William J. Stoffel REG # 39,390/

William J. Stoffel

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Computer file info: cs03-036--suppl-Cert-of-Correction.doc file size: 56832

Appendix

- **certificate of correction form (SB44) (submitted in duplicate)**
- Copy of pages 1 thru 12 of Applicant's reply to the office action dated June 2, 2005 (Ex parte Quayle).

PTO/SB/44 (04-05)
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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,064,358 B2

APPLICATION NO.: 10/743,596

ISSUE DATE : Jun. 20, 2006

INVENTOR(S) : Manna, Indrajit et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In issued Claim 1, Col. 8, line 15, please replace "p-well" with -- N-well -- before "functioning".

In issued Claim 9, Col. 8, line 58, please replace "grounded-sate" with -- grounded-gate -- before "nMOS".

In issued Claim 14, Col. 9, line 16, please add -- pad -- after "first I/O".

In issued Claim 14, Col. 9, line 22, please replace "p-well" with -- N-well -- after "the deep".

In issued Claim 20, Col. 9, line 50, please replace "fanning" with -- forming -- before "a RC network".

In issued Claim 20, Col. 10, line 24, please replace "p-well" with -- N-well -- before "functioning".

In issued Claim 33, Col. 11, line 4, please replace "p-well" with -- N-well -- before "functioning".

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,064,358 B2

APPLICATION NO.: 10/743,596

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INVENTOR(S) : Manna, Indrajit et al.

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In issued Claim 33, Col. 11, line 4, please replace "p-well" with -- N-well -- before "functioning".

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FAX information
Note : 11 total pages in this fax

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Subject:

Docket CS03-036
S/N 10/743,596
Response to Office action dated 2005-06-02
File date: 2003-12-22
Inventor: Indrajlt Manna
Title: **TRIGGERERD BACK-TO-BACK DIODES FOR ESD PROTECTION IN TRIPLE-WELL CMOS PROCESS**

Group Art Unit: 2811
Examiner: Owens, Douglas W

RESPONSE TO OFFICE ACTION

Dear Sirs:

This is in response to the Office action dated 06/02 /2005, please consider the following remarks:

CERTIFICATE OF MAILING OR FACSIMILE TRANSMISSION

I hereby certify that this correspondence is being :
[x_] FAXED to the central facsimile number of patent and trademark office at the following number 703) 872-9306 or
[__] deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450,
on the date below.
Signature _____ Date 6/22/05
William J. Stoffel Reg. No. 39,390 Customer number 30402

This response to Office Action has the following sections:

- **Amendments to the Claims** are reflected in the listing of claims that begin on the next page.
- **Remarks/Arguments** begin on the page following the amendments to the claims.

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listing, of claims in the application:

Listing of claims:

1. (CURRENTLY AMENDED) A ESD protection device comprising:

a) a n-doped region and a p-doped region in a p-well in a semiconductor structure; said n-doped region and said p-doped region are spaced;

b) a n-well and a deep n-well surrounding said p-well on the sides and bottom;

c) a first I/O pad connected to said n-doped region;

d) a trigger circuit connected to said first I/O pad and said p-doped region;

e) a second I/O pad connected to said n-well;

f) a parasitic bipolar transistor is comprised of the n-doped region functioning as a collector terminal, the P-well functioning as a base terminal, and the deep N-well functioning as the emitter terminal; whereby under an ESD condition, the p-well is charged positive using the trigger circuit and said parasitic bipolar transistor can be turned on.

2. (ORIGINAL) The ESD protection device of claim 1 which further comprises:

a first gate over said p-well between said n-doped region and said p-doped region; and

a second gate over said p-well between said p-doped region and said n-well.

3. (ORIGINAL) The ESD protection device of claim 1 which further comprises:

a first gate over said p-well between said n-doped region and said p-doped region; and

a second gate over said p-well between said p-doped region and said n-well;

said second I/O pad connected to said first gate and said second gate.

4. (ORIGINAL) The ESD protection device of claim 1 which further comprises said n-doped region and said p-doped region are separated by an isolation region.

5. (ORIGINAL) The ESD protection device of claim 1 wherein said trigger circuit comprises a chain of diodes.

6. (ORIGINAL) The ESD protection device of claim 1 wherein said trigger circuit comprises a RC network comprised of a diode connected to a resistor and said p-doped region; said resistor connected to said second I/O pad.

7. (ORIGINAL) The ESD protection device of claim 1 wherein said trigger circuit comprises a RC network comprised of a diode connected to a resistor and said p-doped region; said resistor connected to said second I/O pad; said RC network has a RC time constant about 10 times the duration of human body model ESD waveform.

8. (ORIGINAL) The ESD protection device of claim 1 wherein said trigger circuit comprises a RC network comprised of a diode connected to a resistor and said p-doped region; said resistor connected to said second I/O pad; said RC network has a RC time constant between about 1.5 and 2 micro seconds.

9. (ORIGINAL) The ESD protection device of claim 1 wherein said trigger circuit comprises a grounded–gate nMOS transistor and a resistor connected to the grounded–gate nMOS transistor and to said second I/O pad.

10. (ORIGINAL) The ESD protection device of claim 1 which further includes a N-doped ring region laterally surrounding said p-doped region whereby said N-doped ring region and said deep n-well increase the resistance of the parasitic bipolar transistor thereby increasing the pinch off during an ESD event.

11. (ORIGINAL) The ESD protection device of claim 1 wherein said semiconductor structure is comprised of silicon.

12. (PREVIOUSLY PRESENTED) The ESD protection device of claim 1 which further includes contacts to said n-doped and said p-doped regions; said contacts are comprised of a silicide.

13. (ORIGINAL) The ESD protection device of claim 1 wherein said ESD protection device is further comprised of a second parasitic bipolar transistor.

14. (CURRENTLY AMENDED) A method of forming an ESD protection device comprising:

a) forming a n-doped region and a p-doped region in a p-well in a semiconductor structure; said n-doped region and said p-doped region are spaced;

b) forming a n-well and a deep n-well that surround said p-well on the sides and bottom;

c) connecting electrically a first I/O pad to said n-doped region;

d) connecting electrically a trigger circuit to said first I/O pad and said p-doped region;

e) connecting electrically a second I/O pad to said n-well; whereby a parasitic bipolar transistor is comprised of the n-doped region functioning as a collector terminal, the P-well functioning as a base terminal, and the deep N-well functioning as the emitter terminal; whereby under an ESD condition, the p-well is charged positive using the trigger circuit and the parasitic bipolar transistor can be turned on.

15. (ORIGINAL) The method of claim 14 which further comprises;

forming a first gate over said p-well between said n-doped region and said p-doped region; and

forming a second gate over said p-well between said p-doped region and said n-well;

electrically connecting said first gate, said second gate and second I/O pad.

16. (ORIGINAL) The method of claim 14 which further comprises:

forming a first gate over said p-well between said n-doped region and said p-doped region; and

forming a second gate over said p-well between said p-doped region and said n-well.

17. (ORIGINAL) The method of claim 14 which further includes forming isolation regions separating said n-doped region and p-doped region.

18. (ORIGINAL) The method of claim 14 wherein said trigger circuit is formed by forming a chain of diodes.

19. (ORIGINAL) The method of claim 14 which further includes forming said trigger circuit by forming a RC network comprised of a diode connected to a resistor and said p-doped region; said resistor connected to said second I/O pad.

20. (PREVIOUSLY PRESENTED) The method of claim 14 which further includes forming said trigger circuit by forming a RC network comprised of a diode connected to a resistor and said p-doped region; said resistor connected to said second I/O pad; said RC network has a RC time constant about 10 times the duration of Human body model ESD waveform.

21. (ORIGINAL) The method of claim 14 which further includes forming said trigger circuit by forming a RC network comprised of a diode connected to a resistor and said p-doped region; said resistor connected to said second I/O pad; said RC network has a RC time constant between about 1.5 and 2 micro seconds.

22. (ORIGINAL) The method of claim 14 which further includes forming said trigger circuit by forming a grounded–gate nMOS transistor and a resistor connected to the grounded–gate nMOS transistor and to the second I/O pad.

23. (ORIGINAL) The method of claim 14 which further includes forming a N-doped ring region laterally surrounding said p-doped region whereby said N-doped ring region and said deep n-well increase the resistance of the parasitic bipolar transistor thereby increasing the pinch off during an ESD event.

24. (ORIGINAL) The method of claim 14 wherein said semiconductor structures comprised of silicon.

25. (ORIGINAL) The method of claim 14 which further includes forming contacts comprised of a silicide to the n-doped regions and said p-doped regions.

26. (CURRENTLY AMENDED) A method for using an ESD protection device comprising the steps of:

(1) providing:

a) a n-doped region and a p-doped region in a p-well in a semiconductor structure; said n-doped region and said p-doped region are spaced;

b) a n-well and a deep n-well surrounding said p-well on the sides and bottom;

c) a first I/O pad connected to said n-doped region;

d) a trigger circuit connected to said first I/O pad and said p-doped region;

e) a second I/O pad connected to said n-well;

f) a parasitic bipolar transistor is comprised of the n-doped region functioning as a collector terminal, the P-well functioning as a base terminal, and the deep N-well functioning as the emitter terminal;

(2) charging said p-well using the trigger circuit under an ESD condition and turning on said parasitic bipolar transistor.

27. (ORIGINAL) The method of claim 26 which further comprises:

forming a first gate over said p-well between said n-doped region and said p-doped region; and

forming a second gate over said p-well between said p-doped region and said n-well.

28. (ORIGINAL) The method of claim 26 which further comprises;

forming a first gate over said p-well between said n-doped region and said p-doped region; and

forming a second gate over said p-well between said p-doped region and said n-well;

connecting said second I/O pad to said first gate and said second gate.

29. (ORIGINAL) The method of claim 26 wherein said trigger circuit is comprised of a chain of diodes.

30. (ORIGINAL) The method of claim 26 wherein said trigger circuit comprises a RC network comprised of a diode connected to a resistor and said p-doped region; said resistor connected to said second I/O pad.

31. (ORIGINAL) The method of claim 26 wherein said trigger circuit comprises a grounded–gate nMOS transistor and a resistor connected to the grounded–gate nMOS transistor and to said second I/O pad.

32. (ORIGINAL) The method of claim 26 which further includes forming a N-doped ring region laterally surrounding said p-doped region whereby said N-doped ring region and said deep n-well increase the resistance of the parasitic bipolar transistor thereby increasing the pinch off during an ESD event.

33. (CURRENTLY AMENDED) A method of using a ESD protection device comprising the steps of :

(1) providing:

a) a n-doped region and a p-doped region in a p-well in a semiconductor structure; said n-doped region and said p-doped region are spaced;

b) a n-well and a deep n-well surrounding said p-well on the sides and bottom;

c) a first I/O pad connected to said n-doped region;

d) a trigger circuit connected to said first I/O pad and said p-doped region;

e) a second I/O pad connected to said n-well;

f) a parasitic bipolar transistor is comprised of the n-doped region functioning as a collector terminal, the P-well functioning as a base terminal, and the deep N-well functioning as the emitter terminal; whereby under an ESD condition, the p-well is charged positive using the trigger circuit and said parasitic bipolar transistor can be turned on;

g) a N-doped ring region laterally surrounding said p-doped region whereby said N-doped ring region and said deep n-well increase the resistance of the parasitic bipolar transistor thereby increasing the pinch off during an ESD event;

(2) reverse-biasing said N-doped ring region during an ESD event to increase the effective resistance seen by the injected current in the P-doped region by said trigger circuit into p-well.

REMARKS/ARGUMENTS

Examiner Owens is thanked for the thorough Office Action.

In the claims

The claims are amended as discussed below. No new matter is added.

Restriction

Applicant gratefully acknowledges the withdrawal of the restriction requirement.

Claim objections

Objection to Claim 3

The objection to claim 3 is acknowledged. I could not find an instance of "sccond" in the original patent application or the previous response to office action. The applicant intends to spell the word as "second". My copies of the previous office action and the application as originally filed show the correct spelling of "second" in claim 3. Possibly, the fax of the previous office action had defect over that word.

Applicant respectfully requests the examiner make an examiner amendment if a correction is required.

Objections to claims 1 and 14, and 26 and 33

Claims 1 and 14, and 26 and 33 are amended as kindly suggested by the examiner.

ALLOWABLE SUBJECT MATTER

The allowance of claims 1-33 is gratefully acknowledged.

Pending claims

It is believed that all the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not bee expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper. and the amendment of any claim does not necessarily signify concession of the unpatentability of the claim prior to its amendment.

CONCLUSION

In conclusion, issuance of the application is requested.

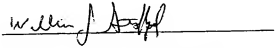
It is requested that the Examiner telephone the undersigned attorney at (215) 670-2455 should there be anyway that we could help to place this Application in condition for Allowance.

Charge to Deposit Account

referencing this attorney docket. The Commissioner is also authorized to charge any additional fee under 37 CFR §1.16 and 1.17 to this Deposit Account.

Respectfully submitted,

Date: 6/22/05



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******* END OF FAX – LAST PAGE ******

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